REMARKS

Claims 1-19 and 24-30 are pending in the present application. By this response, claims 2, 5, 14, 25-28 have been amended and claims 29 and 30 are new. Support for the amendments can be found throughout the specification, drawings and originally filed claims. The amendments therefore present no new matter. Reconsideration and allowance are respectfully requested.

I. Examiner's Request for Additional Prior Art References

The Examiner has requested that Applicants make a query as to any references known to qualify as prior art under 35 U.S.C. sections 102 or 103. A query has been made and no prior art found is sufficient to fulfill the request.

II. Title of the Invention

The Examiner has requested that Applicants submit a new title that is indicative of the claimed invention. Applicants have amended the title accordingly.

III. Claim Rejections

Claims 1-28 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,119,222 to Shiell et al. Applicants traverse this rejection and respectfully assert that Sheill does not disclose all of the claimed limitations.

With specific regard to claim 1, 14, 24 and 26, Shiell fails to provide for searching a cache system at a first level for an *instruction* and searching the cache system at a second level *for the instruction in parallel* with the first level as claimed. Rather, Shiell teaches fetching a branch instruction from the first level of a cache and prefetching either the *target* of the branch instruction or a *later instruction* in the code sequence, where the later instruction has involved a cache miss.

For example, Shiell explicitly states that each branching instruction initiates "one or more prefetches in combination with the fetch of the next instruction (either the next sequential address or the branch target, depending upon the prediction)" (Column 14, lines 16-21). In either case, the prefetched instruction is a different instruction from the fetched instruction. Indeed, it is clear from the discussion in Shiell that the term "expected cache misses" applies to

instructions other than the branch instruction that is fetched from the first level. See, for example, the statement in Shiell that the target addresses of prefetches "are determined by *subsequent instructions* in the pipeline" (Column 10, lines 55-60, emphasis added). See also Shiell's teaching that "prefetches are associated with branching instructions for *later instructions*... that involve cache misses" (Column 16, lines 60-63). For at least the above reasons claims 1, 24 and 26 are not anticipated by Shiell. Claims 2-13, 15-19, 25, 27 and 28 depend from claims 1, 14, 24 and 26, and therefore also recite patentable subject matter. Accordingly, Applicants request that the Examiner withdraw the instant rejection.

Claims 2-13, 15-19, 21-23, 25, 27 and 28 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Shiell. Applicants traverse this rejection and assert that Shiell fails to satisfy a prima facie case of obviousness because all of the claimed limitations are not taught or suggested by the reference.

At the outset, Applicants point out that the rejected claims depend from claims 1, 14, 24 and 26, and therefore include the limitations not found in Shiell as already discussed. Furthermore, there is no motivation to modify Shiell to provide for searching a cache system at a first level for an *instruction* and searching the cache system at a second level *for the instruction in parallel* with the first level as claimed because Shiell demonstrates no appreciation for the approach whatsoever. With specific regard to the rejected claims, Applicants seasonably challenge the Examiner's reliance upon Official Notice and respectfully request a citation of references establishing the alleged common knowledge of all claim features not shown in Shiell as well as evidence of motivation to combine such references with Shiell to arrive at the claimed invention. For example, Applicants assert that receiving a front end re-start instruction as recited in claim 10 is not taught or suggested by Shiell or by common knowledge in the art. For at least the above reasons, the rejected claims recite patentable subject matter. As such, Applicants request that the Examiner withdraw the instant rejection.

IV. New Claims

With regard to new claims 29 and 30, Applicants point out that Shiell is limited to prefetching instructions "into lower levels of cache" and demonstrates no appreciation for

decoding prefetched instructions and providing them to an execution core as claimed (See, Column 6, lines 41-45). Accordingly, claims 29-31 also recite patentable subject matter.

CONCLUSION

Applicants assert that all claims are in condition for allowance. Applicants respectfully request the Examiner to pass this case to issue at the Examiner's earliest possible convenience.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at 703.633.0962.

Respectfully submitted,

Date: 3/19/04

B. Delano Jordan
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Intel Americas, Inc.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on:

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